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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/508,776	09/23/2004	Yoshimasa Okabe	2004_1456A	7891
513	7590	02/21/2008	EXAMINER	
WENDEROTH, LIND & PONACK, L.L.P. 2033 K STREET N. W. SUITE 800 WASHINGTON, DC 20006-1021			WOLDEMARIAM, AKILILU K	
		ART UNIT	PAPER NUMBER	
		2624		
		MAIL DATE	DELIVERY MODE	
		02/21/2008	PAPER	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/508,776	OKABE, YOSHIMASA	
	<b>Examiner</b>	<b>Art Unit</b>	
	Aklilu K. Woldemariam	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 17 December 2007.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 8-11 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 8-11 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 16 August 2007 is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### ***Response to Amendment***

1. *Applicant's amendment filed on December 17, 2007 has been entered. Claims 1-7 have been cancelled. Claims 8-11 have been added. Claims 8-11 are still pending, with claims 8 and 10 being independent.*

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 8-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Inoue et al. (U.S. Patent Publication number 20002/0113885A1).

Regarding claims 8 and 10, *Inoue discloses an image processing apparatus and an image processing method (see fig. 5, image processing signal and image processing circuit and memory control unit) comprising:*

*an image storage unit operable to store an image as a plurality of lines, each line having a plurality of pieces of pixel data sequentially arranged (see item 22, fig. 5 and column 6, line 37-column 7, line 7, image storage referred to memories and pixel data sequentially referred to F1\_1 to F1\_8 and F2\_1 to F2\_8);*

a first reading out unit operable to sequentially read out, from said image storage unit, the plurality of pieces of pixel data of each line of the plurality of lines and operable to sequentially output the plurality of pieces of pixel data sequentially read out (see item 12, fig.5 and column 6, line 64-column 7, line 7 and *pixel data sequentially referred to F1\_1 to F1\_8 and F2\_1 to F2\_8*);

a second reading out unit operable to read out one or more pieces of pixel data located at a head of each line of the plurality of lines and operable to output the one or more pieces of pixel data read out (see column 7, lines 47-61, *head of each line of the plurality of lines referred to the next horizontal period, the FIFO memories from F1\_1 to F1\_8*); and

an arithmetic unit operable to execute an arithmetic process for generating output pixel data using the pixel data output from the first reading out unit and the second reading out unit, wherein (see item 26, fig.5 and column 6, lines 64-67, *arithmetic unit referred to memory control unit*):

before the arithmetic unit completes the arithmetic process for generating a last output pixel data for one of the plurality of lines using the pixel data output from the first reading out unit, the second reading out unit is operable to read out the one or more pieces of the pixel data located at the head of a next line (see fig.7 and column 7, line 62-column 8, line 18, *arithmetic unit completes the arithmetic process for generating a last output pixel data referred to read out in parallel (simultaneously)*); and

the arithmetic unit is operable to use the pixel data output from the second reading out unit when executing the arithmetic process for generating a first output pixel

data for the next line (see *fig. 7 and column 7, line 62-column 8, line 18, arithmetic unit completes the arithmetic process for generating a last output pixel data referred to read out in parallel (simultaneously)*).

Regarding claims 9 and 11, *Inoue discloses the image processing apparatus and the image processing method of claims 8 and 10, wherein the first reading out unit further comprises:*

*a line memory operable to store at least the plurality of pieces of the pixel data belonging to one line of the plurality of lines see item 12, fig. 5 and column 6, line 64-column 7, line 7 and pixel data sequentially referred to F1\_1 to F1\_8 and F2\_1 to F2\_8); and*

*a plurality of registers operable to store the sequentially arranged plurality of pieces of pixel data by sequential shifting (see item 22, column 7, lines 3-7, sequential shifting referred to F1\_1 to F1\_8 or F2\_1 to F2\_8).*

#### ***Response to Arguments***

4. *Applicant's arguments filed on December 17, 2007 have been respectfully considered, but they are not persuasive. Regarding 35 U.S.C. 102 rejection of claim inventions, applicant argued that with reference (*Inoue*) does not disclose the claim inventions. However, Examiner disagreed because regarding claims 8 and 10, *Inoue discloses an image processing apparatus and an image processing method (see fig. 5, image processing signal and image processing circuit and memory control unit) comprising:**

an image storage unit operable to store an image as a plurality of lines, each line having a plurality of pieces of pixel data sequentially arranged (see item 22, fig.5 and column 6, line 37-column 7, line 7, image storage referred to memories and pixel data sequentially referred to F1\_1 to F1\_8 and F2\_1 to F2\_8);

a first reading out unit operable to sequentially read out, from said image storage unit, the plurality of pieces of pixel data of each line of the plurality of lines and operable to sequentially output the plurality of pieces of pixel data sequentially read out (see item 12, fig.5 and column 6, line 64-column 7, line 7 and pixel data sequentially referred to F1\_1 to F1\_8 and F2\_1 to F2\_8);

a second reading out unit operable to read out one or more pieces of pixel data located at a head of each line of the plurality of lines and operable to output the one or more pieces of pixel data read out (see column 7, lines 47-61, head of each line of the plurality of lines referred to the next horizontal period, the FIFO memories from F1\_1 to F1\_8); and

an arithmetic unit operable to execute an arithmetic process for generating output pixel data using the pixel data output from the first reading out unit and the second reading out unit, wherein (see item 26, fig.5 and column 6, lines 64-67, arithmetic unit referred to memory control unit):

before the arithmetic unit completes the arithmetic process for generating a last output pixel data for one of the plurality of lines using the pixel data output from the first reading out unit, the second reading out unit is operable to read out the one or more pieces of the pixel data located at the head of a next line (see fig.7 and column 7, line

*62-column 8, line 18, arithmetic unit completes the arithmetic process for generating a last output pixel data referred to read out in parallel (simultaneously)); and*

*the arithmetic unit is operable to use the pixel data output from the second reading out unit when executing the arithmetic process for generating a first output pixel data for the next line (see fig. 7 and column 7, line 62-column 8, line 18, arithmetic unit completes the arithmetic process for generating a last output pixel data referred to read out in parallel (simultaneously)).*

Regarding claims 9 and 11, *Inoue discloses the image processing apparatus and the image processing method of claims 8 and 10, wherein the first reading out unit further comprises:*

*a line memory operable to store at least the plurality of pieces of the pixel data belonging to one line of the plurality of lines see item 12, fig. 5 and column 6, line 64-column 7, line 7 and pixel data sequentially referred to F1\_1 to F1\_8 and F2\_1 to F2\_8); and*

*a plurality of registers operable to store the sequentially arranged plurality of pieces of pixel data by sequential shifting (see item 22, column 7, lines 3-7, sequential shifting referred to F1\_1 to F1\_8 or F2\_1 to F2\_8).*

### **Conclusion**

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aklilu k. Woldemariam whose telephone number is 571-270-3247. The examiner can normally be reached on Monday-Thursday 6:30 a.m.-5:00 p.m EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Samir Ahmed can be reached on 571-272-7413. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

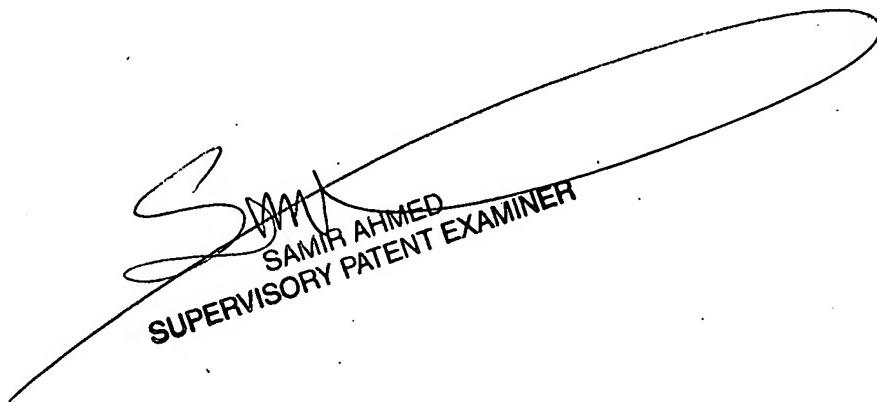
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Samir Ahmed  
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Art Unit 2624

A.W.  
02/15/2008



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